REMARKS/ARGUMENTS

After the foregoing Amendment, Claims 1, 3-12, 14-23, and 25-36 are currently pending in this application. Claim 13 is canceled without prejudice. Claims 7, 12, 14-20, 27, and 32 are amended.

Allowable Subject Matter

The Examiner is thanked for indicating that claims 8, 19, and 33 contain allowable subject matter if written in independent form.

Claim Objections

The Examiner objected to claims 13 and 27. In view of the foregoing amendments, the objection is now moot. The Examiner also objected to claims 8, 9, and 33 because they are dependent upon a rejected base claim. The withdrawal of the objection to the claims 8, 19, and 33 is respectfully requested.

Claim Rejections - 35 USC § 112

Claims 7, 18, and 32 are rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Corrective amendments to claims

7, 18 and 23 obviate these rejections and thus, withdrawal of the 35 USC § 112 rejection is respectfully requested.

Claim Rejections - 35 USC §103(a)

Claims 23, 25, 26, 31, 34, 35, and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,859,878 to Phillips et al. (hereinafter Phillips) and U.S. Patent No. 6,373,902 to Park et al. (hereinafter Park) further in view of U.S. Patent No. 5,768,695 to Fischer et al. (hereinafter Fischer). Claims 1, 3, 4, 6, 9-15, 17, 20-22, and 27-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Philips, Park and Fischer, further in view of U.S. Patent No. 5,761,532 to Yarch et al. (hereinafter Yarch). Finally, claims 5, 16, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,532,533 to Bhandal et al. (hereinafter Bhandal). Applicants respectfully disagree.

Claim 23 recites "a radio interface for interfacing between an analog radio module and a digital module, the interface comprising: a serial bus processor, a programmable radio interface processor (RIP), and a plurality of lookup tables indexed by data received from the analog radio module wherein data values retrieved from the lookup tables may be used to generate processed data for controlling the digital module and the RIP includes at least one memory-mapped register coupled to the serial bus processor."

In contrast, Phillips discloses a software programmable common receive module (PCRM) for receiving IF signals and producing a serial bit stream (*see Phillips Abstract*). More specifically, Phillips discloses a programmable common digital radio that provides an integrated solution for many different types of multi-function communication, navigation, and identification (CNI) suites (col. 2, lines 38-42).

Phillips does not disclose a radio interface for interfacing between an analog radio and a digital module. In contrast, Phillips discloses a PCRM comprising an analog submodule and a digital submodule (col. 7, lines 36-38). Moreover, Phillips merely discloses a tune bus that connects the digital submodule of the PCRM to the analog submodule of the PCRM as disclosed in column 8, lines 21 – 28:

> A <u>tune bus **228** connects the digital submodule **106** of the PCRM **100** (via the digital processing portion **106*b***) to the analog submodule **104** of the PCRM **100**</u>. Further, although not shown, those of skill in the art can utilize the programmability of the hardware described herein and include additional interconnections between the digital processing portion **106*b*** of the digital submodule **106** of the PCRM **100** to the analog submodule **104** of the PCRM **100**.

Nowhere in the above citations, nor anywhere in Phillips, is "a radio interface for interfacing between an analog radio module and a digital module" disclosed or remotely suggested.

In addition, Phillips fails to disclose "a programmable radio interface (RIP) processor." Paragraph [0026] of the current specification discloses:

> <u>The RIP 127 provides configuration control over the interface between analog radio module 138 and digital module 136.</u> Through one or more MMR(s) 133, the RIP 127 controls various functionalities of the interface, such as a chip counter 109, the serial bus processor 120, GPIO registers 124, and data path control (TX IDATA 151, TX QDATA 153, RX IDATA 155, and RX QDATA 157). The RIP 127 can write to bits in an MMR(s) 133 location that enable (change) the format of TX and/or RX data. The data format may be changed to support binary or twos complement format (invert MSB). In turn, the RIP 127 may be controlled by an external processor over a microprocessor bridge 108. Microprocessor bridge 108 provides a mechanism for allowing external processors to control the RIP 127.

The Examiner believes that the air interface unit (AIU) disclosed in Phillips is equivalent to the programmable RIP disclosed in claim 23. However, the AIU disclosed in Phillips merely sends RF (analog) signals to the PCRM (col. 8, lines 29-32).

Further, as the Examiner notes, Phillips fails to disclose a plurality of lookup tables which are indexed by data received from the analog radio module, wherein the data values retrieved from the plurality of lookup tables may be used to generate processed data for controlling the digital module. However, the Examiner believes that Park discloses the above referenced lookup tables. Park discloses a device for linearizing a transmitter in a digital radio communication system. Although, Park discloses predistortion lookup tables, the lookup tables in Park fail to disclose the indexing scheme as disclosed in claim 23. The lookup tables in Park merely reads and outputs predistortion filter coefficient as disclosed in column 7, lines 52-65:

> The I-channel lookup table **351** stores the predistortion values determined by measuring in advance the distortion caused by the I-channel data and the changes of the transmission power and the surrounding temperature of the transmitter. Similarly, the Q-channel lookup table **353** stores the predistortion values determined by measuring in advance the distortion caused by the Q-channel data and the changes of the transmission power and the surrounding temperature of the transmitter. The I-channel lookup table **351** reads and outputs the I-channel predistortion filter coefficient IPDD according to the I-channel address IADDR. Similarly, the Q-channel lookup table **353** reads and outputs the Q-channel predistortion filter coefficient QPDD according to the Q-channel address QADDR.

In contrast, the lookup tables of the present specification are indexed via at least one TPC word, and an AGC word as disclosed in paragraphs [0022] and [0023] of the current specification. Moreover, Park fails to disclose using data values retrieved from the lookup tables to generate processed data for controlling the digital module. Rather, Park discloses the filter coefficient generator generating filter coefficients IFC and QFC for controlling the filter coefficients for the I-channel and Q-channels, respectively, according to the predistortion data IPDD and QPDD received from the memory (col. 5, lines 30-36).

As the Examiner notes, Phillips as modified by Park, does not disclose that the radio interface processor includes at least one memory-mapped register. However, the Examiner believes Fisher discloses a register set. Fischer discloses an apparatus for providing a flexible interface for creating the necessary control signaling of a radio transmitter. This disclosure

includes a radio interface unit and a register set coupled to a state machine. Although, as the Examiner notes, the combination of Fischer, Phillips and Park does not teach or, suggest the use of memory-mapped registers, the Examiner, citing U.S. Patent No. 5,933,158 to Santos (hereinafter "Santos"), has suggested that it would have been obvious to one of skill in the art to use "memory mapped" registers as they are the fastest registers. However, the Applicants respectfully submit that the advantage gained in speed is also not disclosed in Santos. In fact, a close reading of Santos shows that the speed Advantage is actually achieved by the processor memory accesses and not the system of memory-mapped registers.

Therefore, Phillips, Park, and Fischer, alone or in combination, fail to teach or suggest the method disclosed in claim 23. Applicants believe the claim to be distinguishable over the cited references.

Claims 25-36 are dependent upon claim 23, and the Applicants believe these claims are allowable over the cited references of record for the same reasons provided above.

Claim 1 is similar to claim 23, and also recites "a programmable radio interface processor (RIP) that includes at least one memory-mapped register configured to control data generated by the serial bus processor..."

Because claim 1 is similar to claim 23, Applicant's believe this claim to be distinguishable over Phillips, Park, and Fischer for the same reasons provided above.

As the Examiner notes, Phillips, Park, and Fischer fail to disclose memory-mapped registers configured to control data generated by the serial bus processor. However, the Examiner believes Yarch discloses said memory-mapped registers. Yarch discloses a direct memory access (DMA) controller, for performing DMA transfers of segments of data between a first bus and a second bus. Yarch, merely discloses a memory-mapped register interface used to program a PCI bus interface and the local bus interface as disclosed in column 3, line 59 to column 4, line 7:

> The DMA controller **306** further includes a first, hereinafter "local," interface **322** coupled to the local memory **314** via the memory controller **312**. The DMA controller **306** also includes a second, hereinafter "PCI," interface **320** couples to the PCI bus **302**. As explained above the PCI bus **302** can be either a primary PCI or a secondary PCI bus depending on which channel of the DMA controller **306** is used. The DMA controller **306** uses direct addressing for both the PCI bus and the local bus **310**. The DMA controller **306** supports data transfers to and from a full 64-but address range of the PCI bus **302**. The PCI interface **320** supports unlimited burst lengths. The local bus interface **322** supports 2 kilobyte burst transfers. <u>PCI bus interface and the local bus interface can be programmed from the local bus **310** through a memory-mapped register interface.</u> Each channel can be programmed independently and has its own set of registers.

In contrast, the current specification recites in paragraphs [0026] and [0027]:

> The RIP 127 provides configuration control over the interface between analog radio module 138 and digital module 136. <u>Through one or more MMR(s) 133, the RIP 127 controls various functionalities of the interface, such as a chip</u>

> counter 109, the serial bus processor 120, GPIO registers 124, and data path control (TX IDATA 151, TX QDATA 153, RX IDATA 155, and RX QDATA 157). The RIP 127 can write to bits in an MMR(s) 133 location that enable (change) the format of TX and/or RX data. The data format may be changed to support binary or twos complement format (invert MSB). In turn, the RIP 127 may be controlled by an external processor over a microprocessor bridge 108. Microprocessor bridge 108 provides a mechanism for allowing external processors to control the RIP 127.
>
> Operation of the serial bus processor 120 is controlled by one or more memory-mapped registers (MMR(s)) 133. The MMR(s) 133 are accessed by a finite state machine(FSM) 131 internal to the RIP 127, and may also be accessed via a processor interface, external to the RIP 127. In order to determine the precise timing of external events, and also to command and control various radio operations, the RIP 127 accepts a clock signal from a chip counter 109.

Hence, Yarch fails to disclose writing "to bits in an MMR(s) location that enable (change) the format of TX and/or RX data. Therefore, Phillips, Park, Fischer, and Yarch, alone or in combination, fail to teach or suggest the method disclosed in claim 23. Applicants believe the claim to be distinguishable over the cited references.

Claim 12 is rejected for similar reasons as Claim 1, and the Applicants believe Claim 12 is allowable for the same reasons provided above.

Claims 3-11 and 14-22 are dependent upon claims 1 and 12 respectfully, and the Applicants believe these claims are allowable over the cited references of record for the same reasons provided above.

In view of the foregoing amendment, rejection of claim 13 is now moot.

Based on the arguments presented above, withdrawal of the 35 U.S.C. §103(a) rejection of claims 1, 3-12, 14-23, and 25-36 is respectfully requested.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephonic interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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Enclosure